Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	300	(substrate and (IC integrated near2 circuit chip wafer semiconductor silicon die dice chip) and (pheripheral sidewall side) and lead and (coat$4 mask$4 overlay$4 seal$4 lay$4 top$4 wrap$4 cover$4) and pad).clm.	US-PGPUB	OR	ON	2005/08/11 09:48
L2	2245	(257/676).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/11 09:48
L3	358	(257/674).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/11 09:48
L4	466	(257/673).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/11 09:48
L5	1735	(257/690).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/11 09:48
L6	3647	(257/787).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/11 09:48
L7	635	(257/790).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/11 09:48
L8	1259	(438/123).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/11 09:48
L9	1004	(438/125).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/11 09:48

L10	928	(438/124).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/11 09:48
L11	12	L2 and (pheripheral sidewall side) with (coat$4 mask$4 overlay$4 seal$4 lay$4 top$4 wrap$4 cover$4) near3 pad	US-PGPUB	OR	ON	2005/08/11 09:48
L12	8	L3 and (pheripheral sidewall side) with (coat$4 mask$4 overlay$4 seal$4 lay$4 top$4 wrap$4 cover$4) near3 pad	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/11 09:48
L13	12	L4 and (pheripheral sidewall side) with (coat$4 mask$4 overlay$4 seal$4 lay$4 top$4 wrap$4 cover$4) near3 pad	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/11 09:48
L14	68	L5 and (pheripheral sidewall side) with (coat$4 mask$4 overlay$4 seal$4 lay$4 top$4 wrap$4 cover$4) near3 pad	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/11 09:48
L15	88	L6 and (pheripheral sidewall side) with (coat$4 mask$4 overlay$4 seal$4 lay$4 top$4 wrap$4 cover$4) near3 pad	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/11 09:48
L16	10	L7 and (pheripheral sidewall side) with (coat$4 mask$4 overlay$4 seal$4 lay$4 top$4 wrap$4 cover$4) near3 pad	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/11 09:48
L17	34	L9 and (pheripheral sidewall side) with (coat$4 mask$4 overlay$4 seal$4 lay$4 top$4 wrap$4 cover$4) near3 pad	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/11 09:48
L18	64	L8 and (pheripheral sidewall side) with (coat$4 mask$4 overlay$4 seal$4 lay$4 top$4 wrap$4 cover$4) near3 pad	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/11 09:48

L19	254	L11 L12 L13 L14 L15 L16 L17 L18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/11 09:48